

Serial No.: 10/796,426	Confirmation No.: 1895	Art Unit: 2183
-------------------------------	------------------------	----------------

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Brian Robert Prasky	Date:	13 December 2008
Serial No.:	10/796,426	Art Unit:	2183
Filing Date:	9 March 2004	Examiner:	Brian P. Johnson
Confirmation No.:	1895	Docket No.:	POU920030068US1
Title:	Method, System and Program Product for a Pipelined Processor Having a Branch Target Buffer (BTB) to Create a Recent Entry Queue in Parallel with the Branch Target Buffer (BTB)	Attorney:	Graham S. Jones, II 42 Barnard Avenue Poughkeepsie, NY 12603-5023

SUPPLEMENTAL AMENDMENT CORRECTING NON-COMPLIANT AMENDMENT

The Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Your Honor:

In response to the Office Action of 13 November 2008, please amend the above-identified application as follows:

Amendments to the Title	begin on page	2	of this paper.
Amendments to the Abstract	begin on page	3	of this paper
Amendments to the Specification	begin on page	4	of this paper
Amendments to the Claims	begin on page	21	of this paper.
Remarks/Arguments	begin on page	27	of this paper.